REMARKS

Claims 1, 2 and 4-22 are pending in this application. Claims 1, 7, 10, 21 and 22 are independent claims. By this amendment: claims 1 and 4-9 are amended; claim 3 is canceled; and new claims 21 and 22 are added. Reconsideration in view of the above amendments and following remarks is respectfully solicited.

I. ALLOWABLE SUBJECT MATTER

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 10-20 over the art of record.

The Office Action also asserts that claims 5, 6 and 8 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended to overcome the rejection under 35 U.S.C. §112, 2nd paragraph.

Applicants respectfully submit that new claim 21 includes the limitation of claim 6 and original claim 1 and new claim 22 includes the limitation of claim 8 and original claim 7. As such, claims 21 and 22 are also allowable. In addition, applicants respectfully submit that all of claims 1, 2, and 4-22 are allowable, for at least the reasons set forth below.

II. THE CLAIMS SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, 2nd PARAGRAPH

The Office Action rejects claims 3-9 under 35 U.S.C. §112, 2nd paragraph. This rejection is respectfully traversed.

Applicants respectfully submit that the amendments to claims 4-9 obviates the rejection of claim 3-9 under 35 U.S.C. §112, 2nd paragraph.

Accordingly, withdrawal of the rejection of claims 3-9 under 35 U.S.C. §112, 2nd paragraph is respectfully solicited.

III. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by Applicants' Prior Art Figure 19 and the Admitted Prior Art in the disclosure of page 5. This rejection is respectfully traversed.

Applicants respectfully submit that cited Figure 19 and the admitted prior art in the disclosure of page 5 of applicants' specification fails to teach or suggest each and every feature as set forth in the claimed invention.

In a semiconductor device of the claimed invention, the electrical properties of the semiconductor element changes so that the element fails to operate properly when the semiconductor element becomes unleveled. Thus, in this configuration it is possible to protect the semiconductor element from any type of circuit analysis once detached or unleveled, and hence secrets can be concealed.

Moreover, the claimed configuration is arranged such that when the semiconductor element is detached from the board, the element is subjected to a predetermined level of stress, causing the element to deform. Thus, the leakage of secrets from the semiconductor design (unmounted element) once detached can be prevented.

In contrast, in the admitted prior art on page 5 of applicants' specification, a semiconductor element is not secured with stress level so that the element deforms when detached from the board. As such, in contrast to the present invention, it is

very easy to carry out circuit analysis of the prior art element once removed from the board.

According to MPEP §2131, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claims." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913 (Fed. Cir. 1989). The elements must be arranged as required by the claims, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicants respectfully submit that the Office Action has failed to establish the required *prima facie* case of anticipation because the cited admitted prior art fails to teach or suggest each and every feature as set forth in the claimed invention.

Applicants respectfully submit that independent claims 1, 7, 21 and 22 are allowable over the admitted prior art for at least the reasons noted above.

As for each of the dependent claims not particularly discussed above, these claims are also allowable for at least the reasons set forth above regarding their corresponding independent claims, and/or for the further features claimed therein.

Accordingly, withdrawal of the rejection of claims 1 and 2 under 35 U.S.C. §102(e) is respectfully solicited.

IV. CONCLUSION

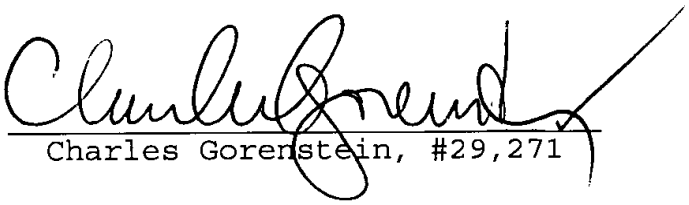
In view of the foregoing, Applicants respectfully submit that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Carolyn T. Baumgardner (Reg. No. 41,345) at (703) 205-8000 **to schedule a Personal Interview**.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment from or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, the extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASH & BIRCH, LLP

By 
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CG/CTB/mpe
1248-0538P

Attachment: Version with Markings to Show Changes Made

VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) A semiconductor device, in which a semiconductor element with an integrated circuit is secured to a board,

wherein the semiconductor element is secured in a level position and specified to operate normally only when the semiconductor element is maintained in this level position,

wherein the semiconductor element is secured with such a stress level applied on a back thereof that when the semiconductor element is detached from the board, the semiconductor element at least partially deforms due to the stress.

4. (Amended) The semiconductor device as defined in claim [3] 1,

wherein the semiconductor element has a thickness of 50 μm or less in the area where the semiconductor element is [processed] secured.

5. (Amended) The semiconductor device as defined in claim [3] 1,

wherein the semiconductor element is specified to include a transistor section wherein transistors are provided at high density, the transistor section at least partially deforming convexly or concavely due to the stress when detached from the board.

6. (Amended) The semiconductor device as defined in claim 1,

wherein the semiconductor element includes detector means for detecting an electrical property developing [in a level part] only when the semiconductor element is level, so as to control operation of the integrated circuit.

7. (Amended) A method of manufacturing a semiconductor device, comprising,

[after] securing a semiconductor element [with] having an integrated circuit to a board so as to be level with the board,

[the step of processing] securing at least a part of a back of the semiconductor element to the board so as to develop [such] a stress level that reacts when the semiconductor element is detached from the board, causing at least a part [thereof deforms] of the semiconductor element to deform, wherein the semiconductor element operates normally only when the semiconductor device is level.

8. (Amended) The method of manufacturing a semiconductor device as defined in claim 7,

wherein the [processing] securing at least a part of a back step is specified to be carried out by at least one technique selected from [the] a group consisting of scraping by means of dicing, sand blast, and sandpaper and treatment by means of laser beam projection.

9. The method of manufacturing a semiconductor device as defined in claim 7,

wherein the [processing] securing step [is specified to render] results in the semiconductor element [have] having a

thickness of 50 μm or less where the semiconductor element is [processed] secured.

New claims 21 and 22 are added.